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EXAMINER	
WON, MICHAEL YOUNG	
ART UNIT	PAPER NUMBER
2155	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/767,405	SHANBHAG ET AL.	
	Examiner	Art Unit	
	MICHAEL Y. WON	2155	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-117* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-117* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/22/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the Amendment filed April 3, 2008.

2. Claims 1-117 have been examined and are pending with this action.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-117 are rejected under 35 U.S.C. 102(b) as being anticipated by Stai et al. (US 6,401,128).

INDEPENDENT:

As per **claim 1**, Stai teaches a data switching device for connecting to a series of nodes and to a first fabric, the device comprising:

a plurality of fabric ports for coupling to the series of nodes (see Fig.1);

at least one node port for connecting to the first fabric (see Fig.1); and

a switch coupled to said plurality of fabric ports and said at least one node port for interconnecting said ports (see Fig.1 and col.3, lines 57-62: “Fabric 102 comprises plurality of switches associated with ports 104A, 104B, and 105 that internally connect

the ports such that data into one port of the switch can be output from any of the other ports").

As per **claim 9**, Stai teaches a Fibre Channel switch for connecting to a series of nodes and to a first fabric, the switch comprising:

a plurality of F__ports for coupling to the series of nodes (see Fig.1);

at least one N__port for connecting to the first fabric (see Fig.1); and

a switch circuit coupled to said plurality of F__ports and said at least one N_port for interconnecting said ports (see Fig.1 and col.3, lines 57-62: "Fabric 102 comprises plurality of switches associated with ports 104A, 104B, and 105 that internally connect the ports such that data into one port of the switch can be output from any of the other ports").

As per **claim 17**, Stai teaches a network comprising:

a series of nodes (see Fig.1);

a first fabric (see Fig.1 and col.3, lines 54-57); and

a data switching device connected to said series of nodes and to said first fabric, said device including:

a plurality of fabric ports coupled to said series of nodes (see Fig.1);

at least one node port connected to said first fabric (see Fig.1); and

a switch coupled to said plurality of fabric ports and said at least one node port for interconnecting said ports (see Fig.1 and col.3, lines 57-62: "Fabric 102 comprises plurality of switches associated with ports 104A, 104B, and 105 that

internally connect the ports such that data into one port of the switch can be output from any of the other ports").

As per **claim 28**, Stai teaches a network comprising:

a series of nodes (see Fig.1);

a first fabric (see Fig.1 and col.3, lines 54-57); and

a Fibre Channel switch connected to said series of nodes and to said first fabric, said switch including:

a plurality of F_ports coupled to said series of nodes (see Fig.1);

at least one N_port connected to said first fabric (see Fig.1); and

a switch circuit coupled to said plurality of F_ports and said at least one N_port for interconnecting said ports (see Fig.1 and col.3, lines 57-62: "Fabric 102 comprises plurality of switches associated with ports 104A, 104B, and 105 that internally connect the ports such that data into one port of the switch can be output from any of the other ports").

As per **claim 39**, Stai further teaches a network comprising:

a series of nodes, each having two ports (see Fig.1);

a first fabric (see Fig.1 and col.3, lines 54-57); and

two data switching devices, each connected to one port of each of said series of nodes and to said first fabric, each said device including:

a plurality of fabric ports coupled to said one port of said series of nodes (see Fig.1);

at least one node port connected to said first fabric (see Fig.1); and

a switch coupled to said plurality of fabric ports and said at least one node port for interconnecting said ports (see Fig.1 and col.3, lines 57-62: "Fabric 102 comprises plurality of switches associated with ports 104A, 104B, and 105 that internally connect the ports such that data into one port of the switch can be output from any of the other ports").

As per **claim 50**, Stai teaches a network comprising:

a series of nodes, each having two ports (see Fig.1);

a first fabric (see Fig.1 and col.3, lines 54-57); and

two Fibre Channel switches connected to one port of each of said series of nodes and to said first fabric, each said switch including:

a plurality of F_ports coupled to said one port of said series of nodes (see Fig.1);

at least one N_port connected to said first fabric (see Fig.1); and

a switch circuit coupled to said plurality of F__ports and said at least one N_port for interconnecting said ports (see Fig.1 and col.3, lines 57-62: "Fabric 102 comprises plurality of switches associated with ports 104A, 104B, and 105 that internally connect the ports such that data into one port of the switch can be output from any of the other ports").

As per **claim 61**, Stai teaches a network comprising:

a series of nodes, each having two ports (see Fig.1);

first and second fabrics (see Fig.1 and col.3, lines 54-57); and

two data switching devices, each connected to one port of each of said series of nodes and to said first and second fabrics, each said device including:

a plurality of fabric ports coupled to said one port of said series of nodes (see Fig.1);

two node ports, one connected to each of said first and second fabrics (see Fig.1); and

a switch coupled to said plurality of fabric ports and said two node ports for interconnecting said ports (see Fig.1 and col.3, lines 57-62: "Fabric 102 comprises plurality of switches associated with ports 104A, 104B, and 105 that internally connect the ports such that data into one port of the switch can be output from any of the other ports").

As per **claim 71**, Stai teaches a network comprising:

a series of nodes, each having two ports (see Fig.1);

first and second fabrics (see Fig.1 and col.3, lines 54-57); and

two Fibre Channel switches connected to one port of each of said series of nodes and to said first and second fabrics, each said switch including:

a plurality of F_ports coupled to said one port of said series of nodes (see Fig.1);

two N_ports, one connected to each of said first and second fabrics (see Fig.1); and

a switch circuit coupled to said plurality of F_ports and said two N_ports for interconnecting said ports (see Fig.1 and col.3, lines 57-62: "Fabric 102

comprises plurality of switches associated with ports 104A, 104B, and 105 that internally connect the ports such that data into one port of the switch can be output from any of the other ports").

As per **claim 81**, Stai teaches a network comprising:

a series of nodes, each having two ports (see Fig.1);

first and second fabrics (see Fig.1 and col.3, lines 54-57); and

two data switching devices, each connected to one port of each of said series of nodes and to one of said first and second fabrics, each said device including:

a plurality of fabric ports coupled to said one port of said series of nodes (see Fig.1);

two node ports connected to one of said first and second fabrics (see Fig.1); and

a switch coupled to said plurality of fabric ports and said two node ports for interconnecting said ports (see Fig.1 and col.3, lines 57-62: "Fabric 102 comprises plurality of switches associated with ports 104A, 104B, and 105 that internally connect the ports such that data into one port of the switch can be output from any of the other ports").

As per **claim 91**, Stai teaches a network comprising:

a series of nodes, each having two ports (see Fig.1);

first and second fabrics (see Fig.1 and col.3, lines 54-57); and

two Fibre Channel switches connected to one port of each of said series of nodes and to one of said first and second fabrics, each said switch including:

a plurality of F__ports coupled to said one port of said series of nodes (see Fig.1);

two N_ports connected to one of said first and second fabrics (see Fig.1); and

a switch circuit coupled to said plurality of F_ports and said two N_ports for interconnecting said ports (see Fig.1 and col.3, lines 57-62: "Fabric 102 comprises plurality of switches associated with ports 104A, 104B, and 105 that internally connect the ports such that data into one port of the switch can be output from any of the other ports").

As per **claim 101**, Stai teaches a method for routing between a series of nodes and a first fabric using a data switching device, the method comprising:

providing a plurality of fabric ports on the device coupled to the series of nodes (see Fig.1);

providing at least one node port on the device connected to the first fabric (see Fig.1); and

interconnecting said plurality of fabric ports and said at least one node port with the device (see Fig.1 and col.3, lines 57-62: "Fabric 102 comprises plurality of switches associated with ports 104A, 104B, and 105 that internally connect the ports such that data into one port of the switch can be output from any of the other ports").

DEPENDENT:

As per **claims 2, 10, 18, 29, 40, 51, 62, 72, 82, 92, and 102**, which respectively depend on claims 1, 9, 17, 28, 39, 50, 61, 71, 81, 91, and 101, Stai further teaches wherein said at least one node port (N_port) operates as a virtual node port (see col.3, lines 64-66), with one virtual node address for each of said plurality of fabric ports (F_ports) connected to nodes (see col.3, lines 62-64).

As per **claims 5, 13, 21, 32, 43, 54, 65, 75, 85, 95, and 103**, which respectively depend on claims 1, 9, 17, 28, 39, 50, 61, 71, 81, 91, and 101, Stai teaches further comprising:

at least one intermediate port coupled to said switch (switch circuit), wherein said switch routes frames between said plurality of fabric ports (F_ports) and said at least one node port (N_port) through said at least one intermediate port (see col.2, lines 5-7).

As per **claims 6, 14, 22, 33, 44, 55, 66, 76, 86, 96, and 104**, which respectively depend on claims 5, 13, 21, 32, 43, 54, 65, 75, 85, 95, and 103, Stai further teaches wherein the interconnection between said at least one intermediate port and either said plurality of fabric ports (F_ports) or said at least one node port (N_port) is a private interconnection and said at least one intermediate port and said other port perform public to private and private to public address translations (see col.2, lines 11-15).

As per **claims 7, 15, 23, 34, 45, 56, and 105**, which respectively depend on claims 5, 13, 21, 32, 43, 54, 103, Stai further teaches wherein the number of intermediate ports equals the number of node ports (N_ports) (see col.1, line 67-col.2, line 2).

As per **claims 8, 16, 24, 35, 46, 57, 67, 77, 87, 97, and 106**, which respectively depend on claims 1, 9, 17, 28, 39, 50, 61, 71, 81, 91, and 101, Stai further teaches wherein said switch performs public to private and private to public address translations between said plurality of fabric ports (F_ports) and said at least one node port (N_port) (see col.2, lines 11-15).

As per **claims 25, 36, 47, 58, 68, 78, 88, and 98**, which respectively depend on claims 17, 28, 39, 50, 61, 71, 81, and 91, Stai further teaches wherein said nodes are host computers (see col.3, lines 64-66).

As per **claims 107-117**, which respectively depend on claims 1, 9, 17, 28, 39, 50, 61, 71, 81, 91, and 101, Stai further teaches wherein said plurality of fabric ports (F_ports) form a second fabric (see col.3, lines 56-57).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3-4, 11-12, 19-20, 30-31, 41-42, 52-53, 63-64, 73-74, 83-84, and 93-94 rejected under 35 U.S.C. 103(a) as being unpatentable over Stai et al. (US 6,401,128) in view of Reamer (US 2003/0229780).

As per **claims 3, 11, 19, 30, 41, 52, 63, 73, 83, and 93**, which respectively depend on claims 1, 9, 17, 28, 39, 50, 61, 71, 81, and 91, Stai does not explicitly teach wherein said switch (switch circuit) is further adapted to act as a firewall.

Reamer teaches wherein said switch (switch circuit) is further adapted to act as a firewall (see page 3, [0050]).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the system of Stai in view of Reamer so that said switch (switch circuit) is further adapted to act as a firewall. One would be motivated to do so because Stai teaches of providing communication between private loop devices and public devices and such implementation would do so without compromising security.

As per **claims 4, 12, 20, 31, 42, 53, 64, 74, 84, and 94**, which respectively depend on claims 1, 9, 17, 28, 39, 50, 61, 71, 81, and 91, Stai does not explicitly teach wherein said switch (switch circuit) is further adapted for intrusion detection.

Reamer teaches wherein said switch (switch circuit) is further adapted for intrusion detection (see page 1, [0014]).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the system of Stai in view of Reamer so that said switch (switch circuit) is further adapted for intrusion detection. One would be motivated to do so because Stai teaches of providing communication between private loop devices and public devices and such implementation would do so without compromising security.

5. Claims 26-27, 37-38, 48-49, 59-60, 69-70, 79-80, 89-90, and 99-100 rejected under 35 U.S.C. 103(a) as being unpatentable over Stai et al. (US 6,401,128) in view of Chatterjee (US 7,103,704).

As per **claims 26, 37, 48, 59, 69, 79, 89, and 99**, which respectively depend on claims 25, 36, 47, 58, 68, 78, 88, and 98, Stai does not explicitly teach wherein said host computers are blade computers and are located in a blade server chassis.

Chatterjee teach wherein said host computers are blade computers and are located in a blade server chassis (see col.1, lines 35-42).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the system of Stai in view of Chatterjee so that host computers are blade computers and are located in a blade server chassis. One would be motivated to do so because Stai teaches that the device is any computer or peripheral which is coupled or attached to the fabric (see col.3, line 64-col.4, line 5).

As per **claims 27, 38, 49, 60, 70, 80, 90, and 100**, which respectively depend on claims 26, 37, 48, 59, 69, 79, 89, and 99, Stai does not explicitly teach wherein said data switching device is a blade located in said blade server chassis.

Chatterjee teach wherein said data switching device is a blade located in said blade server chassis.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the system of Stai in view of Chatterjee so that data switching device is a blade located in said blade server chassis. One would be

motivated to do so because such implementation allows for improved processing and recovery from a single point of failure.

Response to Arguments

6. Applicant's arguments filed April 3, 2008 have been fully considered but they are not persuasive.

In response to applicant's arguments regarding claims 1, 9 and 101, the respective recitation “A data switching device for connecting…”, “A Fibre Channel switch for connecting…”, and “A method for routing between…”; has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951). For this reason, the broad limitations of claims 1, 9, and 101 are explicitly taught by Stai.

Regarding the argument of claims 17, 28, 39 and 50, the applicant(s) argue that because Fig.1 was cited to teach the component elements of the claims, "this leaves no remaining elements in Fig.1 to be corresponded to the remaining claim element. Although Fig.1 does not explicitly show the remaining elements, Stai teaches the “Fabric 102 comprises plurality of switches associated with ports 104A, 104B, and 105 that internally connect the ports such that data into one port of the switch can be output

from any of the other ports" (see col.3, lines 57-62). The applicant(s) seem to be asserting that the examiner intends Fig.1 to teach all elements of the recited claims. This assertion is improper.

Again with respect to the arguments regarding independent claims 61, 71, 81 and 91, and dependent claims 5-8, 13-16, 21-24, 32-35, 43-46, 54-57, 65-67, 75-77, 85-87, 95-97 and 103-106, the applicant(s) make similar assertions as above. This too is an improper assertion. Other citations have been provided to teach the limitations not found in Fig.1.

In response to the argument of claims 2, 10, 18, 29, 40, 51, 62, 72, 82, 92, and 102, the examiner equates the N_Port to a virtual node port, because Stai teaches that the "N_Port is a label" (see rejection above).

Conclusion

7. For the reasons above, claims 1-117 have been rejected and remain pending.

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL Y. WON whose telephone number is (571)272-3993. The examiner can normally be reached on M-Th: 10AM-8PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Saleh Najjar can be reached on 571-272-4006. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Michael Won/
Primary Examiner
May 28, 2008